Electronics Summary

- **Voltage** is a measure of electrical potential energy
- **Current** is moving charge caused by voltage
- **Resistance** reduces current flow
  - Ohm’s Law: $V = I R$
- **Power** is work over time
  - $P = I V = I^2 R = V^2/R$
- **Capacitors** store charge
  - It takes time to charge/ discharge a capacitor
  - Time to charge/discharge is related exponentially to $RC$
  - It takes energy to charge a capacitor
  - Energy stored in a capacitor is $(1/2)CV^2$
Reminder: Voltage Division

- Find the voltage across any series-connected resistors

\[ V_X = \frac{R_X}{R_{\text{tot}}} V_S \]

Example of Voltage Division

- Find the voltage at point A with respect to GND

\[ V_X = \frac{R_X}{R_1 + R_2} V \]
Example of Voltage Division

- Find the voltage at point A with respect to GND

\[
V_X = \frac{R_X}{R_1 + R_2} V
\]

\[
V_1 = \frac{900}{1000} \times 5v = 4.5v
\]

\[
V_2 = \frac{100}{1000} \times 5v = 0.5v
\]

So, \( V_{A,GND} = 0.5v \)

\[
V_1 = \frac{100}{1000} \times 5v = 0.5v
\]

\[
V_2 = \frac{900}{1000} \times 5v = 4.5v
\]

So, \( V_{A,GND} = 4.5v \)

---

How Does This Relate to VLSI?

- Recall the voltage division example:
  - Consider what we could do if we had a device that we could switch from high resistance to low resistance
  - We could use it to force A high or low depending on the relative resistance of the elements

- This is a transistor:
  - Specifically a CMOS FET
  - Complementary Metal-Oxide Semiconductor Field Effect Transistor
  - If voltage on Gate is high, then there is a low-resistance between Source and Drain, otherwise it's a very high-resistance

---
Model of a CMOS Transistor

Switch Level Model

Switch is closed if Gate voltage is high

Switch is open if Gate voltage is low

\[ R_{on} = \text{Some resistance in FET itself} \]

\[ C_G = \text{Capacitance of the gate} \]

Two Types of CMOS Transistors

- **N-type transistor**
  - High voltage on Gate connects Source to Drain
  - Passes 0 well, passes 1 poorly

- **P-type transistor**
  - Low voltage on Gate connects Source to Drain
  - Passes 1 well, passes 0 poorly
CMOS Transistors

- Complementary Metal Oxide Semiconductor
- Two types of transistors
  - Built on silicon substrate
  - “majority carrier” devices
  - Field-effect transistors
    - An electric field attracts carriers to form a conducting channel in the silicon…
    - We’ll get much more of this later…
    - For now, just some basic abstractions

Silicon Lattice

- Transistors are built on a silicon substrate
- Silicon is a Group IV material
- Forms crystal lattice with bonds to four neighbors

Figures from Reid Harrison
3D lattice…

“Semi” conductor?

- Thermal energy (atomic-scale vibrations) can shake an electron loose
  - Leaves a “hole” behind

Figures from Reid Harrison
“Semi” conductor?

- Room temperature: $1.5 \times 10^{10}$ free electrons per cubic centimeter
  - But, $5 \times 10^{22}$ silicon atoms / cc
  - So, one out of every 3 trillion atoms has a missing e

Dopants

- **Group V:** extra electron (n-type)
  - Phosphorous, Arsenic,

- **Group III:** missing electron, (p-type)
  - Usually Boron

Figures from Reid Harrison
Dopants

- Note that each type of doped silicon is electrostatically neutral in the large
  - Consists of mobile electrons and holes
  - And fixed charges (dopant atoms)

p-n Junctions

- A junction between p-type and n-type semiconductor forms a diode.
  - Current flows only in one direction
p-n Junctions

- Two mechanisms for carrier (hole or electron) motion
  - Drift - requires an electric field
  - Diffusion – requires a concentration gradient

Figures from Reid Harrison

p-n Junctions

- With no external voltage diffusion causes a depletion region
  - Causes an electric field because of charge recombination
  - Causes drift current…

Figures from Reid Harrison
**p-n Junctions**

- Eventually reaches equilibrium where diffusion current offsets drift current

By applying an external voltage you can modulate the width of the depletion region and cause diffusion or drift to dominate...

Figures from Reid Harrison
N-type Transistor

Poly Gate
Gate Oxide
Diffusion

Drain
Gate
Source
N+ N+
P-doped substrate

Body is commonly tied to ground (0 V)

When the gate is at a low voltage:
- P-type body is at low voltage
- Source-body and drain-body diodes are OFF
- No current flows, transistor is OFF

nMOS Operation

- Body is commonly tied to ground (0 V)
- When the gate is at a low voltage:
  - P-type body is at low voltage
  - Source-body and drain-body diodes are OFF
  - No current flows, transistor is OFF
**nMOS Operation Cont.**

- When the gate is at a high voltage:
  - Positive charge on gate of MOS capacitor
  - Negative charge attracted to body
  - Inverts a channel under gate to n-type
  - Now current can flow through n-type silicon from source through channel to drain, transistor is ON
pMOS Transistor

- Similar, but doping and voltages reversed
  - Body tied to high voltage ($V_{DD}$)
  - Gate low: transistor ON
  - Gate high: transistor OFF
  - Bubble indicates inverted behavior

A Cutaway View

- CMOS structure with both transistor types
Transistors as Switches

- For now, we’ll abstract away most analog details...

<table>
<thead>
<tr>
<th>G=0</th>
<th>G=1</th>
</tr>
</thead>
<tbody>
<tr>
<td>Good 0</td>
<td>Good 1</td>
</tr>
<tr>
<td>Good 0</td>
<td>Poor 1</td>
</tr>
</tbody>
</table>

Not Perfect Switches!

“Switching Circuit”

- For example, a switch can control when a light comes on or off

+5v  
No electricity can flow  
0v
“AND” Circuit

- Both switch X **AND** switch Y need to be closed for the light to light up

```
+5v
X  Y
0v
```

“OR” Circuit

- The light comes on if either X **OR** Y are closed

```
+5v
X  Y
0v
```
CMOS Inverter

- Consider this connection of transistors
  - If input is at a high voltage, output is low
  - If input is at a low voltage, output is high
- By changing the resistances, it becomes one of two different voltage dividers
  - It’s a voltage inverter!

<table>
<thead>
<tr>
<th>A</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

CMOS Inverter

<table>
<thead>
<tr>
<th>A</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
</tr>
</tbody>
</table>

Input

Output

$V_{DD}$

A

Y

GND
CMOS Inverter

A | Y
---|---
0 | ?
1 | ?

V_{DD}  
A=+5V  
Y=?

CMOS Inverter

A | Y
---|---
0 | ?
1 | 0

GND  
A=1  
Y=0

GND
CMOS Inverter

<table>
<thead>
<tr>
<th>A</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

Timing Issues in CMOS

- Recall that it takes time to charge capacitors
- Recall that the gate of a transistor looks like a capacitor
- Wires have resistance and capacitance also!
Power Consumption

- Power is consumed in CMOS by charging and discharging capacitors
  - Note that there is no static power dissipation in CMOS
  - There’s never a DC path to ground
- Good news:
  - You’re not consuming power unless you’re switching
- Bad news:
  - Switching activity is caused by clock, which is going faster and faster
- If the first-order power effect is capacitor charging/discharging, and the clock causes this:
  \[ P = C V^2 f \]
CMOS NAND Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

A = 0
B = 0
Y = 1

ON
OFF
CMOS NAND Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td></td>
</tr>
</tbody>
</table>

A=0
B=1

A=1
B=0

Y=1

ON
OFF
ON
OFF
CMOS NAND Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Y</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>1</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>0</td>
</tr>
</tbody>
</table>

A=1
B=1

ON
OFF

Y=0

CMOS NOR Gate

<table>
<thead>
<tr>
<th>A</th>
<th>B</th>
<th>Z</th>
</tr>
</thead>
<tbody>
<tr>
<td>00</td>
<td>1</td>
<td></td>
</tr>
<tr>
<td>01</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>10</td>
<td>0</td>
<td></td>
</tr>
<tr>
<td>11</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

A
B

Z
Take a moment and draw what you think the transistor circuit for a 3-input NAND gate should be…
Static CMOS Gate Template

- P-Type pullups and N-Type pulldowns
  - Boolean duals of each other…
  - Note the natural inverting behavior…
    - N-types turn on with high voltages, but pull low
    - P-types turn on with low voltages, but pull high

Pullup Network (PUN)

Pulldown Network (PDN)

Vdd

Inputs

Output

GND

N-type and P-type Uses

- Because of the imperfect nature of the transistor switches
  - ALWAYS use N-type to pull low
  - ALWAYS use P-type to pull high
  - If you need to pull both ways, use them both

S=0, In ≠ Out

S=1, In = Out
Switch to Chalkboard

- Complex Gate
- Tri-State
- Latch
- D-register
- XOR